REMARKS/ARGUMENTS

Reconsideration and allowance of this application are respectfully requested. Currently, claims 1 and 4 are pending in this application.

Rejection Under 35 U.S.C. §103:

Claims 1 and 4 were rejected under 35 U.S.C. §103 as allegedly being unpatentable over Applicant admitted prior art and Shimotashiro et al (U.S. '043, hereinafter "Shimotashiro"). Applicant respectfully traverses this rejection.

In order to establish a prima facie case of obviousness, all of the claim limitations must be taught or suggested by the prior art. The combination of Applicant admitted prior art and Shimotashiro fails to teach or suggest all of the claim limitations. For example, the combination fails to teach or suggest "a temperature characteristic compensating circuit connected to a base of said PNP bipolar transistor and canceling a temperature characteristic of said PNP bipolar transistor; wherein said temperature characteristic compensating circuit includes an NPN bipolar transistor having a conductive terminal connected to the base of said PNP bipolar transistor," as required by independent claim 1. Similarly, the combination fails to teach or suggest "a temperature characteristic compensating circuit for canceling a temperature characteristic of the PNP bipolar transistor, the temperature characteristic compensating circuit including an NPN bipolar transistor having a conductive terminal connected to a base of said PNP bipolar transistor," as required by independent claim 4.

Through the above claimed limitations, a temperature characteristic compensating circuit includes an NPN bipolar transistor having a conductive terminal connected to the base of a PNP bipolar transistor. The temperature characteristic compensating circuit including the NPN bipolar transistor serves to stabilize a collector current of the PNP bipolar transistor against ambient temperature variation, and to cancel the temperature characteristic of the PNP bipolar transistor. (See, e.g., page 2, lines 3-23 and page 6, line 14 to page 7, line 12 of the originally-filed specification).

Fig. 4 (specifically identified by the Office Action) of Shimotashiro discloses a first delay section 32 having an NPN type transistor Q21 and a second delay section 33 having a PNP type transistor Q31. However, Shimotashiro neither teaches nor suggests any temperature characteristic compensation relationship between the first delay section 32 and the second delay section 33. In particular, Shimotashiro neither teaches nor suggests any temperature characteristic compensation of the PNP type transistor Q31 of the second delay section 33 by the NPN type transistor Q21 of the first delay section 32. There is no teaching or suggestion of the NPN type transistor Q21 of the first delay section canceling the temperature characteristic of PNP type transistor Q31. Applicant submits that no such concept is even contemplated by Shimotashiro. For example, it is (if anything) the value I0 (or I1) of current from current source I21 (or I31) connected to the emitter of NPN type transistor Q21 (or PNP type transistor Q31)

which is varied so as to compensate for the temperature characteristic of NPN transistor Q21 (or PNP type transistor Q31).

The interaction between PNP type transistor Q31 and NPN type transistor Q21 is described, for example, in col. 14, lines 5-25 of Shimotashiro which states the following:

> "In the above configuration, when the sinusoidal analog signal is transferred from the input terminal 34 to the base of the transistor Q_{21} as an input signal, the analog signal is amplified in the transistor Q_{21} and is delayed by the function of the first resistor R_{21}, the second resistor R_{22}, the first capacitor C_{21}, and the second capacitor C_{22} in the first delay section 32 of the delay circuit unit 31 before the analog signal delayed is applied to the base of the transistor Q_{31}. Thereafter, the analog signal is again delayed by the function of the third resistor R_{31}, the fourth resistor R_{32}, the third capacitor C_{31}, and the forth capacitor C_{32} in the second delay section 33 of the delay circuit unit 31 before the analog signal delayed is output from the output terminal 36 as an output signal.
>
> In this case, the forward current gains h_{fe} of the transistors Q_{21}, Q_{31} are large enough, and stray capacitance of the delay circuit unit 31 is small enough. Therefore, the analog signal passes through the delay circuit unit 31 without decreasing the amplitude of the analog signal."

In the above passage of Shimotashiro, there is no teaching or suggestion of the PNP type transistor Q31 being temperature compensated by the first delay section 32 having NPN type transistor Q21. Accordingly, Applicant respectfully submits that the combination of Applicant admitted prior art and Shimotashiro fails to teach or suggest all of the claim limitations. Applicant therefore

respectfully requests that the rejection of claims 1 and 4 under 35 U.S.C. §103 be withdrawn.

Conclusion:

Applicant believes that this entire application is in condition for allowance and respectfully requests a notice to this effect. If the Examiner has any questions or believes that an interview would further prosecution of this application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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